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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/043,896 | 01/09/2002 | Kevin K. Lee | 113025-120US2 | 7745 |

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| EXAMINER | |
|---|---|
| WANG, GEORGE Y | |
| ART UNIT | PAPER NUMBER |
| 2871 | |

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/043,896 | LEE ET AL. | |
| | Examiner | Art Unit | |
| | George Y. Wang | 2871 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *28-35 and 39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27,36-38 and 40-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-4, 14-16, 27, 36, and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admission of Prior Art (AAPA) in view of Wojnarowski et al. (U.S. Patent No. 5,737,458, from hereinafter "Wojnarowski").

3. As to claim 1, AAPA discloses an optical chip (pg. 1, lines 17-18) having at least one large mode field size dielectric waveguide (fig. 1; pg. 1, lines 17-18) that interfaces with an external optical device (pg. 1, lines 20-22), at least one low minimum bending radius dielectric waveguide (pg. 2, lines 15-17), and at least one optical function (pg. 1, lines 17-18) connected to the low minimum bending radius dielectric waveguide.

However, AAPA fails to disclose the large mode field size dielectric waveguide, the low minimum bending radius dielectric waveguide, and the optical function being fabricated monolithically on a single substrate.

Wojnarowski discloses an optical chip with dielectric waveguides (col. 2, lines 14-16) and optical function devices (fig. 2, ref. 50, 52) are fabricated monolithically on a single substrate (fig. 2, ref. 54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange a large mode field size dielectric waveguide, a low minimum bending radius dielectric waveguide, and an optical function monolithically on a single substrate since one would be motivated to provide an optimum platform for a high density interconnect structure (col. 1, lines 20-35). This not only provides stability but also high compatibility with many other interconnections, including external waveguides and optical devices (col. 2, lines 61-67).

4. Regarding claims 2-4 and 14-16, AAPA discloses an external optical device that is a low index difference dielectric waveguide, which is edge emitting/receiving, and provides input from an external optical chip (pg. 1, lines 20-22; fig. 1). Furthermore,

AAPA discloses this large mode field size dielectric waveguide, which is also a low index difference dielectric waveguide, having a low index core and cladding that are related by the following expression: $1<([n_1-n_3]/n_3)<0.1$ (fig. 1; pg. 1, line 22 – pg. 2, line 14). AAPA also discloses the low minimum bending radius dielectric waveguide, which is a high index difference dielectric waveguide, having a high index core and cladding that are related by the following expression: $0.1\leq([n_2-n_3]/n_3)$ (pg. 2, lines 15-24).

5. Regarding claims 17-19, AAPA discloses a large mode field size dielectric waveguide having a low index core and cladding that are related by the following expression: $1<([n_1-n_3]/n_3)<0.1$ (fig. 1; pg. 1, line 22 – pg. 2, line 14) and a low minimum bending radius dielectric waveguide i having a high index core and cladding that are related by the following expression: $0.1\leq([n_2-n_3]/n_3)$ (pg. 2, lines 15-24).

However, AAPA fails to disclose a large mode field size dielectric waveguide having a low index core and cladding that are related by the following expression: $0<([n_1-n_3]/n_3)<0.04$ or $0<([n_1-n_3]/n_3)<0.01$ and a low minimum bending radius dielectric waveguide having a high index core and cladding that are related by the following expression: $0.3\leq([n_2-n_3]/n_3)$.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have set the following core and cladding relationships expressed by: $0<([n_1-n_3]/n_3)<0.04$, $0<([n_1-n_3]/n_3)<0.01$, and $0.3\leq([n_2-n_3]/n_3)$. Since AAPA is clear to disclose that there is possible to be in the ranges as recited above (pg. 1, lines 28-30) and since AAPA does not specify any added advantages to have core-cladding

relationships expressed within the constraints of these expressions, one of ordinary skill in the art would recognize that conforming to these expressions is a matter of design and need-based optical applications.

6. As per claim 27, AAPA discloses an optical function device, however, AAPA fails to specifically disclose the optical function device as any structure that performs at least one of generating, modifying, and measuring at least on of the amplitude, frequency, wavelength, dispersion, timing, propagation direction, and polarization properties of one or more light pulses.

Wojnarowski discloses an optical chip with an optical function device (fig. 7, ref. 50, 52) that performs at least one of generating, modifying, and measuring at least on of the amplitude, frequency, wavelength, dispersion, timing, propagation direction, and polarization properties of one or more light pulses (col. 6, lines 58-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to an optical function device that performs at least one of generating, modifying, and measuring at least on of the amplitude, frequency, wavelength, dispersion, timing, propagation direction, and polarization properties of one or more light pulses since one would be motivated to achieve any of these functions on an optical chip. One of ordinary skill in the art would recognize these functions as well known and defined on the basis of performance and function needs.

7. As to claim 36 and 40-42, AAPA discloses the optical chip as recited above with a second chip including an emitting/receiving optical device, which may also be an external large mode field size dielectric waveguide, to optically connect to the large mode size dielectric waveguide of the first chip (pg. 1, lines 20-22).

8. Claims 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Wojnarowski, in view of Hammer (U.S. Patent No. 4,776,720).

AAPA and Wojnarowski disclose the optical chip as recited above with waveguide coupling devices (fig. 7, ref. 72, 74).

However, the references fail to specifically disclose a coupler that couples the low minimum bending radius dielectric waveguide to the large mode field size dielectric waveguide, and which has a first dielectric channel waveguide including a first core material having a first tapered region surrounded by a cladding material, a second dielectric channel waveguide including a second core material having a second tapered region surrounded by the cladding material such that all of the second tapered region being completely embedded within the first tapered region, where a first mode for propagating lightwaves defined by the first dielectric channel waveguide gradually transforms into a second mode defined by the second dielectric channel waveguide. Furthermore, the references fail to teach that the first and second tapered region narrow toward each other and are graded in the horizontal and vertical directions.

Hammer discloses an optical waveguide coupler (fig. 1, ref. 10) that includes a first core material (fig. 1, ref. 18) having a first tapered region (fig. 1, ref. 18a)

surrounded by a cladding material (fig. 1, ref. 16), a second dielectric channel waveguide including a second core material (fig. 1, ref. 20) having a second tapered region (fig. 1, ref. 20a) surrounded by the cladding material such that all of the second tapered region being completely embedded within the first tapered region (fig. 1, ref. 22), where a first mode for propagating lightwaves defined by the first dielectric channel waveguide gradually transforms into a second mode defined by the second dielectric channel waveguide (col. 2, lines 43-60). Furthermore, the reference teaches that the first and second tapered region narrow toward each other (fig. 1, ref. 22) and are graded in the horizontal and vertical directions.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a tapered coupler device as recited above in an optical chip to couple the low minimum bending radius dielectric waveguide to the large mode field size dielectric waveguide since one would be motivated to effective transition the first mode of the large mode field size dielectric waveguide to the second mode of the low minimum bending radius dielectric waveguide (col. 2, lines 43-60). Not only does such a coupler achieve this, but a tapered coupler also allows the coupling of light from waveguides having different specific geometries and materials, such as from various layers to one that has fewer layers, and all the while being able to have controlled coupling precision (col. 1, lines 26-40).

9. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Wojnarowski, in view of Carnevale et al. (U.S. Patent No. 4,412,722, from hereinafter "Carnevale").

AAPA and Wojnarowski disclose the optical chip as recited above with a low minimum bending radius dielectric waveguide (pg. 2, lines 15-17) having a high index core material. However, the references fail to specifically disclose a graded index region between the rough sides of the core and cladding to transition from high to low indices.

Carnevale discloses a low bend radius waveguide with a graded index region (abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a graded index region between the rough sides of the core and cladding to transition from high to low indices since one would be motivated to minimize dispersion and therefore to maximize bandwidth (abstract). Furthermore, improved field confinement adds to the overall lower clad-to-core ratios, lower cabling, microbending, and curvature-induced losses (abstract), which all ultimately serve to information and date transmission of optical communication systems. Furthermore, with respect to claim 26, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

10. Claims 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Wojnarowski, in view of Joannopoulos et al. (U.S. Patent No. 5,955,749, from hereinafter "Joannopoulos").

AAPA and Wojnarowski disclose the optical chip as recited above with a second chip including an emitting/receiving optical device, which may also be an external large mode field size dielectric waveguide, to optically connect to the large mode size dielectric waveguide of the first chip, however, the references fail to specifically disclose the application of an anti-reflective coating on either of the waveguides.

Joannopoulos discloses an optical chip with waveguides that have anti-reflective coatings (col. 1, lines 46-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied anti-reflective coatings to the waveguides since one would be motivated to further reduces optical losses (col. 1, lines 46-48) during transmission between the waveguides.

***Response to Arguments***

11. Applicant's arguments filed 30 June 2003 have been fully considered but they are not persuasive.

With regards to the restriction requirement, Applicant argues that separate between Group I and III is improper because Group III does not have separate utility. First, t is clear that the invention of Group III is a subcombination since a substrate is claimed. Nowhere is it stated how this substrate is to be used. And even if it were

disclosed, the fact that is includes a limitation on the amount of loss ("no more than 1dB of loss), it is clearly differentiated from the invention of Group I. Furthermore, as stated in the previous action, the subcombination has separate utility in semiconductor interconnection, switching, and a variety of other opto-electro applications. Therefore, Examiner maintains the validity of the restriction requirement.

With regards to Claim 26, Applicant's argument to the objection is that the limitation "graded index region reduces scattering loss" does not recite a manner in which the apparatus can be used, but rather that is a structural characteristic "constructed" to "reduces scattering loss." Examiner agrees with Applicant in that a claimed limitation should recite a structural characteristic or be "constructed" to perform some function. However, it is clear that Applicant does not say more than that. Applicant's claimed limitation does not teach anything about a structural construction that "reduces scattering loss." Therefore, the objection is valid. However, since the recitation includes elements not given patentable weight. Examiner has removed the objection and included the reasoning within the rejection for clarity to the rejection.

With regards to Applicant's main argument that AAPA does not disclose an optical chip with "at least one large mode field size dielectric waveguide," "at least one low minimum bending radius dielectric waveguide," and "at least one optical function...connected to the low minumum bending radius waveguide," Examiner asserts that AAPA has not been "mischaracterized."

In AAPA, it is clear that a "at least one large mode field size dielectric waveguide," "at least one low minimum bending radius dielectric waveguide," and "at

least one optical function...connected to the low minumum bending radius waveguide" are disclosed. Applicant argues that the background does not disclose that the optical chips contain low minimum bending radius waveguides and cites p. 2, lines 15-17 as defense. However, Examiner asserts that the reference teaches a high index difference waveguide with a reduced minimum bending radii (lines 23-24). AAPA discloses its drawbacks, but it nevertheless teaches that element.

So in regards to the drawbacks set forth by AAPA, Wojnarowski discloses dielectric waveguides and optical function devices are fabricated monolithically on a single substrate to cure the deficiency. Applicant disagrees with the use of this reference because the Wojnarowski reference does not teach "at least one large mode field size dielectric waveguide," "at least one low minimum bending radius dielectric waveguide," and "at least one optical function...connected to the low minumum bending radius waveguide." Examiner notes that the purpose of the Wojnaroski reference is not to disclose those elements, but to provide teaching and motivation for combining the elements taught in AAPA. If Wojnaroski disclosed "at least one large mode field size dielectric waveguide," "at least one low minimum bending radius dielectric waveguide," and "at least one optical function...connected to the low minumum bending radius waveguide," there would be no reason to include an obviousness rejection. Clearly, as recited in the above rejection, one of ordinary skill in the art at the time the invention was made would have arranged a large mode field size dielectric waveguide, a low minimum bending radius dielectric waveguide, and an optical function monolithically on a single substrate since one would be motivated to provide an optimum platform for a

high density interconnect structure (col. 1, lines 20-35). This not only provides stability but also high compatibility with many other interconnections, including external waveguides and optical devices (col. 2, lines 61-67).

Therefore, Examiner holds to the validity of the references and maintains the rejection.

***Conclusion***

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Y. Wang whose telephone number is 703-305-7242. The examiner can normally be reached on M-F, 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 703-305-3492. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

gw
November 12, 2003